

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
27 December 2002 (27.12.2002)

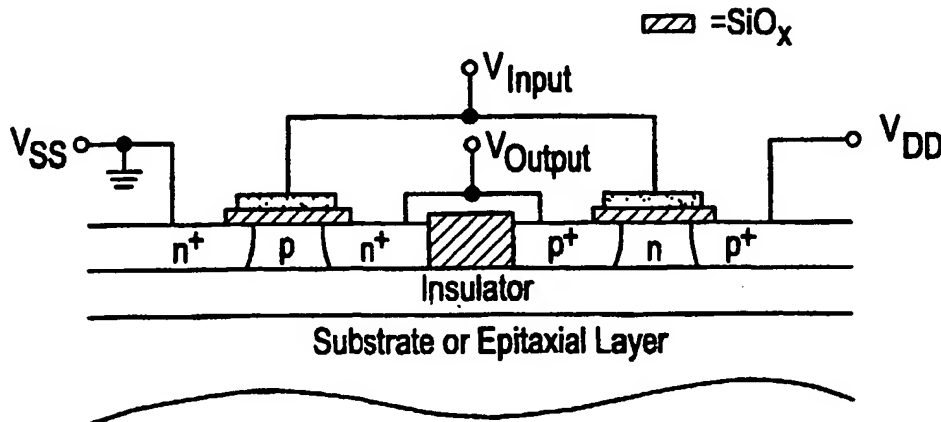
PCT

(10) International Publication Number
WO 02/103767 A1

- (51) International Patent Classification⁷: **H01L 21/20**, 21/36, 21/339, 21/31, 21/469
- (74) Agents: **HANDELMAN, Joseph, H. et al.**; Ladas & Parry, 26 West 61st Street, New York, NY 10023 (US).
- (21) International Application Number: **PCT/US01/40970**
- (22) International Filing Date: 14 June 2001 (14.06.2001)
- (25) Filing Language: English
- (26) Publication Language: English
- (63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 09/188,586 (CON)
Filed on 9 November 1998 (09.11.1998)
- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).
- (71) Applicant (*for all designated States except US*): **NAN-ODYNAMICS, INC.** [US/US]; 510 E. 73rd Street, New York, NY 10021 (US).
- (72) Inventors; and
- (75) Inventors/Applicants (*for US only*): **WANG, Chia-Gee** [US/US]; 44 Glenwood Road, Millwood, NY 10456 (US). **TSU, Raphael** [US/US]; 9327 Willowglen Tr., Charlotte, North Carolina, NC 28215 (US). **LOFGREN, John, Clay** [US/US]; 1230 York Avenue, New York, NY 10021 (US).
- Published:
— with international search report
- For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: EPITAXIAL SiO_x BARRIER/INSULATION LAYER

CMOS - EpiSiO_x /SOI



(57) Abstract: A method for producing an insulating or barrier layer (Fig. 1B), useful for semiconductor devices, comprises depositing a layer of silicon and at least one additional element on a silicon substrate whereby said deposited layer is substantially free of defects such that epitaxial silicon substantially free of defects can be deposited on said deposited layer. Alternatively, a monolayer of one or more elements, preferably comprising oxygen, is absorbed on a silicon substrate. A plurality of insulating layers sandwiched between epitaxial silicon forms a barrier composite. Semiconductor devices are disclosed which comprise said barrier composite.

-1-

EPITAXIAL SiO_x BARRIER/INSULATION LAYER

The invention relates to an insulating layer/barrier for deposition on a silicon substrate and/or epitaxial silicon surface, composites and structures comprising said insulating layer/barrier, method of making the composites and structure, as well as use of

5 the insulating layer/barrier, composites and structures in the construction of improved semiconductor devices, including but not limited to quantum well, tunneling, metal oxide, SOI, superlattice, and three dimensional architecture. The insulating layer/barrier is formed by combining silicon with one or more elements to form an insulating compound of silicon where one of the possible elements is oxygen, forming a layer of SiO_x where

10 $0 < x < 2.0$. The insulating layer structure is produced in such a way to allow for low defect epitaxial silicon to be deposited next to the insulating layer. It further relates to forming a number of such layers sandwiched between epitaxial silicon.

DESCRIPTION OF RELATED ART

1. L. Esaki and R. Tsu, *IBM J. Res. and Dev.* **14**, 61 (1970).
- 15 2. R. Tsu and L. Esaki, *Appl. Phys. Lett.* **22**, 562(1973); LL Chang, L. Esaki and R. Tsu, *ibid* **24** 593 (1974).
3. R. Tsu, *Nature*, **364** 19 (1993).
4. R. Tsu, A. Filios, C. Lofgren, D. Cahill, J. Vannostrand and C.G. Wang, *Solid-State Electronics* Vol. **40**, Nos. 1-8, pp. 221-223, 1996.
- 20 5. R.Tsu, A. Filios, C. Lofgren, J. Ding, Q. Zhang, J. Morais and C. G. Wang, *Proc. 4th Int. Symp. "Quantum Confinement: Nanoscale Materials, Devices, and Systems"*, Edited by M. Cahay, J. P. Leburton, D. J. Lockwood, and S. Bandyopadhyay, (ECS proc. Vol. **97-11**, 1997) p. 341.
6. J. Ding and R. Tsu, *Appl. Phys. Lett.*, **71**, 2124 (1997).
- 25 7. J. Morais, R. Lender, and R. Tsu, to be published, also in Ph.D. Thesis, Unicamp, Brazil, 1996.
8. Inst. Of Semiconductor Physics, Kiev, Ukraine: Preliminary in Litovcheko et al., *JVST*, B15, 439 (1997).
9. G. I. Distler, and B. B. Zvyagin, *Nature*, **212**, 807-809, (1996).
- 30 10. C. A. O. Henning, *Nature*, **227**, 1129-1131 (1970).
11. O. W. Holland, D. Fathy, and D. K. Sadana, *Appl. Phys. Lett.*, **69**, 674 (1996).

12. P.P. van der Ziel et al., *IEEE Q.E.* **22**, 1587(1982).
13. J.W. Matthews and E.E. Blakeslee, *J. Crystal. Growth*, **32**, 265 (1976).
14. G.C. Osborn, *J. Appl. Phys.* **53**, 1586 (1982).
15. E.H. Poindexter & P.J. Caplan, in "*Ins. Films on Semi*," Edited by M. Schulz and M. Pensl, (Springer, Berlin 1981) p. 150.
16. E.H. Nicollian and R. Tsu, US Pat. No. 5,051,786, Sep.24,1991; R. Tsu, E.H. Nicollian, and A. Reisman, *Appl. Phys. Lett.* **55**, 1897(1989).
17. Q.Y. Ye, R. Tsu and E.H. Nicollian, *Phys. Rev. B.*, **44**, 1806 (1991).
18. R. People, *IEEE Q.E.* **22**, 1696(1986).
19. D.G. Deepe et al., *Appl. Phys. Lett.* **51**, 637 (1987).
20. R. Tsu, US Patent 5,216,262 dated June 1, 1993.
21. Nakashima et al, *Proc. IEEE, 1994 Int. SOI Conf.*, 1994.
22. R. Tsu, A. Filios, C. Lofgren, K. Dovidenko, and C.G. Wang, *Electrochemical & Solid-State Lett.* **1** (2) 80-82 (1998).
- 15 For a general review of quantum devices see:
 23. F. Capasso et al. *IEEE, Transaction on Electron Devices* **36**, 2065 (1989).
 24. F. Sols et al., *Appl. Phys. Lett.* **54** 350(1989).
 25. Kwok Ng, *Complete Guide to Semiconductor Devices*, McGraw Hill, 1995.
- 20 26. S. M. Sze, *VLSI Technology*, McGraw-Hill , 1983.

the disclosure of each being incorporated herein by reference.

Silicon dioxide (SiO₂) has been used for many years as an insulating material in semiconductors. It has excellent insulating properties and provides a potential barrier typically of 3.2eV. However, when SiO₂ is grown adjacent to silicon, there is a high mismatch between monocrystalline or epitaxial silicon and the layer of SiO₂ resulting in accumulated stress. These stresses, and therefore strains, cause the SiO₂ to become amorphous preventing the subsequent growth of epitaxial layers. Monocrystalline silicon in the semiconductor industry is available in the form of thin round disks called wafers. These single crystal wafers are produced by growing single crystal ingots from molten silicon which are then sliced and polished into a final "wafer" upon which semiconductor devices and integrated circuits are manufactured. Matthews and Blakeslee⁽¹³⁾ showed that if the thickness of the "strain" layer is thin enough so that the stored strain energy is

-3-

kept below a critical value, a defect-free superlattice is possible for lattice mismatched systems and hence epitaxial silicon can proceed.

In Tsu U.S. Patent 5,216,262, (20), the disclosure of which is incorporated herein by reference, making alternating thin layers of SiO_2 and epitaxial silicon was claimed as a way to make a barrier material adjacent to which epitaxial silicon can be grown with a low number of defects. Although such a barrier is feasible ^(3, 4, 22), the cost of controlling the process to precisely deposit SiO_2 in thin layers adjacent to epitaxial silicon in a superlattice is difficult and expensive.

SILICON ON INSULATOR (SOI)

Current silicon devices are limited by inherent parasitic circuit elements due primarily to junction capacitance and leakage currents. These problems can be addressed for silicon by fabricating silicon devices in a thin epitaxial layer on top of a buried insulator layer, the so-called silicon on insulator (SOI) approach. This approach allows devices to be isolated from the substrate as well as from each other, eliminating the need for structures such as guard-rings, isolation junctions, etc.⁽²⁶⁾

A number of technologies have been developed to place an insulating layer under a layer of low defect silicon which forms the substrate upon which silicon devices are fabricated. This insulating layer reduces the amount of leakage current as well as the junction capacitance thus significantly improving the device performance. Advantages include substantially reduced power consumption, more efficient low-voltage operation, significantly improved speed, radiation hardening and reduced integrated circuit manufacturing costs. These characteristics make SOI wafers well-suited for many commercial applications, including cellular phones, wireless communications devices, satellites, portable and desktop computers, automotive electronics, and microwave systems.

One method of producing SOI wafers is by implanting oxygen ions below the surface of a silicon wafer in sufficient quantity to transform, with proper annealing, a layer of the silicon to silicon dioxide, while maintaining a thin layer of device quality epitaxial silicon at the surface. During implantation of the oxygen ions through the silicon surface, the surface is damaged reducing the quality of the epi-layer upon which devices are fabricated. Annealing can reduce the oxygen inclusion, however it is difficult to reduce the $[O]$ to values below $10^{17}/\text{cm}^3$. The thickness of the insulating layer is very

difficult to control due to the random nature of scattering arising from ion implantation. Also, the ion implantation equipment costs are expensive.

A second method of production is silicon-on-sapphire ("SOS"). In SOS technology, circuitry is constructed in a layer of silicon, which has been deposited on a sapphire substrate. This material has been used in the construction of radiation resistant circuits. However, there are several problems with this material, including large current conduction in the sapphire when exposed to radiation, brittleness causing breakage during integrated circuit fabrication and large mismatches between sapphire and silicon crystal structures. These problems have led to performance and manufacturability limitations.

10 A third method of production involves the bonding of two thin film wafers. In this approach, two bulk silicon wafers, each with a thermally grown oxide layer, are first bonded together to form a silicon/silicon dioxide/silicon wafer. Thin-film bonded wafers are constructed by bonding the two wafers and then thinning one of the two layers. Several alternatives are currently being explored across the industry to perform the subsequent thinning process -- including mechanical polishing, chemical etching; plasma assisted chemical etching, bond and selective etching of porous silicon or an implant-enhanced slicing of the wafer. The bonded wafer approach has the advantage that the buried oxide can be made very uniform and thick. The top silicon layer retains its high quality, achieving uniformity in the thickness of the top silicon layer, however, has proven difficult. Also, the requirement to use two silicon wafers with complex processing has, to date, resulted in a relatively high cost structure for bonded wafers.

QUANTUM WELLS

The p-n homojunction currently widely used in silicon devices has some serious limitations. Typical p-n homojunctions involve long range electrostatic interaction of free charges and are not abrupt. The electrostatic fields are continuous over a distance, which is significantly longer than the DeBroglie wavelength of an electron. It is a scattering dominated structure for electrons. On the other hand heterojunctions are abrupt and analogous to a waterfall where the change in potential is confined to a very short distance. Heterojunctions are the basis of the barriers formed in GaAs/AlGaAs, GaInAs/AlInAs and other so-called III/V compounds from columns 3 and 5 of the periodic chart. The barriers of those heterojunctions derive from chemical bonding, and are short ranged. Typically in p-n homojunctions the continuous voltage changes occur over a distance of

the order of one micron. With a heterojunction this occurs over a distance on the order of 0.5 nanometers, less than one percent the p-n junction distance. As the size of transistors decrease with time, the heterojunction will be ever more important, particularly for quantum well structures.

5 Dr. L. Esaki and Dr. R. Tsu, while working jointly at the IBM research center ^(1,2), envisioned a new type of man made material which could be used to form what they called superlattice barriers and quantum wells to resolve some of the difficulties of the p-n junction. In order to realize these structures in silicon, a "barrier" material is necessary that can be stacked between epitaxial device grade silicon. The present invention
10 describes such a material.

In his patent 5,216,262, ⁽²⁰⁾ R. Tsu proposed a way to build barriers and quantum wells with silicon and SiO₂, which will allow the economical implementation of quantum wells. The invention provided a quantum well structure useful for semi-conducting devices, said structure comprising two barrier regions and a thin epitaxially grown
15 monocrystalline semiconductor material quantum well sandwiched between said barrier regions, each barrier region consisting essentially of alternate strain layers forming a superlattice, each of said layers being thinner than said quantum well and being so thin that no defects are generated. Creating SiO₂ in such thin layers is commercially expensive and probably not viable. The present patent describes a substitute for SiO₂ in this
20 application, which will be referred to as "said barrier".

METAL OXIDE DEVICES

The silicon MOSFET is probably the single most important structure of electronic device.⁽²⁶⁾ A layer of amorphous SiO₂ is typically sandwiched between a metal contact (the gate) and silicon channel region between the source and drain. The lower the
25 interface defect density between the amorphous SiO₂ and epitaxial silicon, the faster is the switching speed and the less power dissipated. Because of the amorphous nature of current SiO₂ layers, the region of the layer near the silicon is filled with defects, reducing the switching speed of the device, apart from the more obvious problem of building epitaxially grown structure beyond the oxide barrier. In his patent 5,216,262 ⁽²⁰⁾ R. Tsu
30 addressed this shortcoming by introducing an insulating layer consisting essentially of alternate strain layers of SiO₂ and Si forming a superlattice, each of said layers being so thin that no defects are generated as a result of the release of stored strain energy. By

reducing the level of defects at this interface between the insulating layer and the channel region of the device the mobility is increased and performance improved. For reasons stated above forming such layers of SiO_2 and Si is expensive. Once again, in this application the "said barrier" described in this patent can be substituted for SiO_2 .

5

TWO DIMENSIONAL SEMICONDUCTOR DEVICES

Currently silicon-based integrated circuits are limited to construction as two-dimensional devices. Once an oxide layer is deposited in a semiconductor device, there is currently no way to grow epitaxial silicon again on top of the oxide layer. Epitaxial silicon is needed if a second layer of devices is to be constructed on top of the first layer.

10 Growing additional layers could provide significant advantages in improving heat dissipation, simplifying interconnections between devices, and significantly reducing the size of an integrated circuit, depending on the number of layers of devices stacked on top of each other, as well as, the means by which they are interconnected.

SILICON DIOXIDE AS A DIELECTRIC MATERIAL

15

When SiO_2 is used as an insulating layer in semiconductor devices there is a capacitance and resistance associated with such a layer. The capacitance is a function of the area of the contact surface, the thickness of the SiO_2 layer and the dielectric constant of the SiO_2 material. Currently the contact area and distance between contacts can be changed affecting the capacitance and hence the RC time constant associated with the

20 SiO_2 insulating layer. However, the SiO_2 dielectric constant is fixed by the properties of SiO_2 and there is virtually no ability to change that property.

Accordingly, it is an object of the present invention to overcome the drawbacks and disadvantages of the above-described insulating layers and heterojunctions used in silicon based semiconductor devices. The present invention allows control over the

25 dielectric constant, as well as, the thickness of said barrier.

FIRST EMBODIMENT: Si/O

The invention provides a method for the formation of a Si/adsorbed-monolayer-of-oxygen (Si/O) as the building block of a barrier to form a repeatable system – a superlattice. This Si/O building block can be grown on a silicon substrate where silicon

30 layers are grown epitaxially adjacent to each monolayer, or less, of adsorbed oxygen where therein is formed monolayers, or less, of adsorbed oxygen sandwiched between thin epitaxially grown silicon layers. Since all transport properties depend on both the

barrier height and barrier width, and since the barrier width is dictated by the Si-O-Si thickness which cannot be changed, the formation of a superlattice by repeating the basic building block accomplishes the desired thickness of the barrier. A relatively thick barrier is used as an insulating layer for devices such as in the use of SOI, and thin barriers are used for most quantum devices.

Silicon growth beyond a barrier structure consisting of thin layer (typically, 1-2 nm) of silicon sandwiched between adjacent layers of adsorbed oxygen up to 100 Langmuir of exposure is epitaxial and almost free of stacking faults as determined in high resolution TEM, transmission electron microscopy (reference 22). The measured barrier height in the conduction band of a double barrier structure with 1.1 nm silicon layer sandwiched between two adsorbed monolayers of oxygen is 0.5eV. The maximum barrier height in the conduction band is probably limited by 1.5eV, half as large as SiO₂, which is 3.2eV. The rationale is that the interface layer consisting of S/O bonds is closer to SiO rather than SiO₂. Since the effectiveness of a barrier depends on both the height and the width of the barrier, to increase the width the basic period, Si/adsorbed O, may be repeated to form a superlattice. A superlattice of Si/O up to nine periods shows excellent epitaxial growth of silicon beyond the superlattice structure, indicating that the major objective has already been accomplished.

The formation of the structure consists of the deposition of silicon by either MBE (Molecular Beam Epitaxy) or CVD (Chemical Vapor Deposition) onto an epitaxial silicon surface with a controlled adsorption of oxygen. The deposition temperature is generally kept below 650°C to limit possible subsequent desorption of the adsorbed oxygen. The exposure to oxygen is at temperatures generally below 500°C to prevent any migration or re-emission of the adsorbed oxygen. Once the superlattice is formed, silicon capping, usually greater than 4nm in thickness, can prevent any degradation. Specifically, the structure measured here is

Si Substrate/ Si(1.1nm)-O(10L)-Si(1.1nm)-(10L)...Si(1.1nm)-O(10L) /epi- Si

Such a structure has exhibited the following:

- The current through this superlattice has been reduced more than four orders of magnitude.

- Epitaxial silicon after the superlattice is virtually free of stacking faults.

These two facts allow the replacement of SOI by this Si/O superlattice for devices

with high speed including high efficiency FET's currently fabricated on SOI.

A definitive theoretical reason for the formation of epitaxy on apparently disordered adsorbed monolayer of oxygen on silicon is still lacking. It may be due to lateral growth through the “holes” in the coverage of the adsorbed oxygen. It may be due to partial screening of the silicon atomic potential by a monolayer of oxygen. More likely, it may be caused by both mechanisms. We now know a third mechanism: The oxygen monolayer at the interface of two silicon surfaces, Si – O – Si, forms an essentially lattice matched system possibly with a slight twist, resulting in a rotational strain, Subsequent silicon deposition serves to define this strain region.

10 SECOND EMBODIMENT: EPISIO_x

The invention also provides a method of introducing oxygen simultaneously during silicon deposition onto a silicon substrate to form a single insulating/barrier layer of silicon and oxygen referred to as EpiSiO_x wherein $0 < x < 2.0$. This structure forms an epitaxial system on silicon in which epitaxial silicon, almost free of defects such as stacking faults and dislocations, can be grown beyond this EpiSiO_x. This system is therefore an ideal replacement of SOI presently available. As before, a relatively thick barrier is used as an insulating layer for devices as is done in SOI, and thin barriers are used for most quantum devices.

A layer of EpiSiO_x has been formed with the following steps:

- All depositions are below 650°C
- Oxygen is introduced during the silicon deposition.

A summary of what has been achieved:

- The silicon growth beyond the EpiSiO_x of thickness below 10nm may be epitaxial with low defect densities below 10⁹ /cm² .
- 25 • The thinner is the EpiSiO_x ; the thinner is the silicon deposition beyond the structure for complete recovery. An example to make the point is for a 2nm EpiSiO_x , only 4nm of silicon is needed to recover the surface reconstruction. Conversely, the thicker is the EpiSiO_x , the thicker is the silicon deposition necessary to recover a perfect silicon surface reconstruction – the appearance of surface reconstruction is used as a
- 30 figure of merit for the recovery of epitaxy.

The following is believed to be a possible basis for the EpiSiO_x . The structure is all along epitaxial and fairly well matched to the silicon lattice. However, there is a twist,

producing a rotational strain (Bond length may be slightly changed, however, it is a minor effect). The newly arrived silicon layer shares this rotational strain until enough silicon has been deposited. By then, most of the strain is pushed out of the silicon and concentrated in the SiO_x layer in much the same way as the usual strain-layer epitaxy.

5

FIRST AND SECOND EMBODIMENT

Further, the invention includes a method of introducing other elements such as N, C, P, S, Sb, As, H, etc., which serve to replace oxygen for forming a barrier structure with silicon. Inclusion of different elements in place of or in addition to oxygen may also serve as a diffusion barrier in gettering, or trapping, other elements. In this regard, the Si/O
10 superlattice and EpiSiO_x may be reinforced by further diffusion of oxygen through the Si capping layer to be trapped by the barrier layers (Nakashima). The benefit is obvious: (a) the cap layer is epitaxial and defect free, serving as an ideal medium for FET devices, and (b) the epitaxial layer may be made thin enough itself to form barriers for quantum wells and for quantum devices such as the RTD, and quantum transistor and the single electron
15 transistor.

This invention further provides a method to adjust (change) the dielectric constant and barrier height of the barrier layers, both Si/O and EpiSiO_x , by controlling the oxygen (or substitute element) content of the barrier. This can be accomplished by adjusting the level of oxygen during simultaneous deposition for EpiSiO_x and controlling the
20 percentage of monolayer oxygen coverage used in Si/O. In the EpiSiO_x the oxygen can further be adjusted during deposition to produce a barrier with a controlled gradient of oxygen content across the barrier thickness. In Si/O this can be accomplished by repeating layers with varying oxygen exposure per layer. As we discussed before that the thicker the layer of epitaxially grown SiO_x , the thicker is the subsequent Si growth for full
25 recovery of epitaxy. Therefore, for thicker barrier requirements, we need to repeat the process, to build up the thickness of the barrier for a given application.

Both Si/O and EpiSiO_x can be fabricated using Molecular Beam Epitaxy (MBE), and in some cases with Chemical Vapor Deposition (CVD) or by any other means known to those familiar with the state of the art.

30 Any of the above combinations of Si/O and/or EpiSiO_x , either individually or in multiple layers, will from hereon be referred to as said barrier.

This invention further provides a Silicon-on-Insulator (SOI) structure where said

barrier is used as the insulator in the SOI with an epitaxial silicon device layer adjacent to this layer. This barrier layer can be used as is or can be enhanced by a high temperature oxidation procedure as described by Nakashima et al. ⁽²¹⁾

The invention provides for quantum devices where said barrier is used as a barrier
5 with silicon to produce Resonant Tunneling Devices (RTD), (Silicon RTD has been experimentally realized by researchers in Inst. Of Semiconductor Physics, Kiev, Ukraine: Preliminary in Litovcheko et al., JVST, B15, 439 (1997)⁽⁸⁾), quantum well devices, single electron field effect transistors (SEFET), etc. It also provides a metal-oxide-semiconductor field-effect transistor (MOSFET) where the gate "oxide" is replaced
10 completely or partially by said barrier. Additionally, this just described MOSFET can have a layer of said barrier just below the channel region of the device to produce a true two-dimensional electron gas between the source and drain thereby enhancing the mobility and performance of the device.

The main advantage of the present invention is that the said barrier allows for the
15 continued epitaxial growth of silicon adjacent to this layer which is substantially defect free. This can be repeated to produce a stack of alternating said barrier and epitaxial device grade silicon in order to form a 3-dimensional structure for producing the 3-dimensional integrated circuits (3D-IC) of the future in silicon (see figure 7). This invention makes it possible to form the active channel, the contacts, and the insulating
20 regions epitaxially. For example, the channel is made with epitaxial silicon on top of the EpiSiO_x with the source and drain by conventional doping. The conventional n+ or p+ doping on top of an insulating layer serves as a gate (there is no need for polysilicon gate contact because the whole structure preserves epitaxy!) This 3D possibility using EpiSiO_x propels the electronic industry into the 21st century!

25 An important aspect of the present invention is the possibility of building a 3D-IC of the future in silicon because all the components can now be built out of this epitaxial system forming barriers, channels, electrical insulation, etc. Such a 3D-IC can circumvent many problems of interconnection, heat dissipation and others. In the immediate future, a high speed, high efficiency, all silicon FET can be better designed
30 with the EpiSiO_x.

Figure 1A is a diagrammatic illustration of a known CMOS.

Figure 1B is a diagrammatic illustration of a CMOS according to the present

invention.

Figure 2A is a schematic illustration of a known RHET.

Figure 2B is a schematic illustration of a RHET according to the present invention.

5 Figure 2C is a schematic illustration of an energy band diagram for Figs. 2A and 2B.

Fig. 3A is a schematic illustration of a known (MIS) TETTRAN.

Fig. 3B is a schematic illustration of a known GaAs TETTRAN.

10 Fig. 3C is a schematic illustration of a TETTRAN according to the present invention.

Fig. 4 is a schematic illustration of a known MOSFET.

Fig. 5 is a schematic illustration of MOSFET according to the present invention.

Fig. 6 is a schematic illustration of the gate region of a MOSFET according to the present invention.

15 Fig. 7 is a schematic illustration of a portion of an IC according to the present invention.

Fig. 8 is a schematic illustration of a composite structure according to the present invention.

20 Figure 1A is a typical CMOS structure ⁽²⁶⁾ while figure 1B is the same structure utilizing said barrier in an SOI approach. As a result, the individual devices are isolated from the substrate as well as each other eliminating the need for isolation wells, guard rings, etc.

Figure 2A is an example of a quantum well structure device called a resonant-tunneling hot-electron transistor (RHET). Figure 2A is a standard RHET device in 25 Gallium Arsenide. Figure 2B is the same structure applied to the present said barrier and silicon. Figure 2C shows the corresponding energy band diagram for these two structures identifying the quantum well region as part of the emitter for this device. ⁽²⁵⁾

Figure 3A illustrates a tunneling device called a Tunnel-emitter Transistor (TETTRAN). Figure 3A shows this device as a metal-insulator-semiconductor (MIS) 30 TETTRAN where electrons tunnel through the thin SiO₂ layer. Figure 3B shows this same structure in GaAs where it would be more precisely referred to as a heterostructure TETTRAN. Finally, figure 3C is this device where said barrier is substituted for the SiO₂

tunneling barrier of fig. 3A (figs. 3A & 3B from ref. 25).

Figure 4 illustrates a conventional MOS structure as can be found in a Metal-oxide-semiconductor field-effect transistor (MOSFET) for example. This is typical of what is found between the gate and channel region of a MOSFET.

5 Figure 5 illustrates a metal-said barrier -semiconductor structure. We will call this final device structure a metal-superlattice-semiconductor field-effect transistor (MSLSFET).

10 Figure 6 illustrates a metal—oxide/said barrier—semiconductor interface, as would be used in the gate region of a field-effect transistor. This provides an improved interface between the silicon and the gate insulation layer while allowing for a thick layer of SiO₂ as usually applied.

Figure 7 illustrates a proposed 3-dimensional chip architecture using said barrier to isolate epitaxial device layers from one another while providing for localized interconnect between layers.

15 Figure 8 illustrates a proposed structure for very low defect epitaxial silicon (E) to be grown on top of an insulating layer (B) of the present invention which is in turn grown on a substrate of single crystal silicon (A). This approach uses multiple thin layers (B) of said barrier to reduce defect production in the total thickness of the insulating layer as opposed to one thick layer. A top "thin" reflection layer (D) of said barrier to further
20 reduce the defects is included ⁽¹³⁾.

The preferred embodiments of the invention provide for four approaches to the structures for an insulating layer or barrier for use in semiconductor devices and methods for producing such structures:

25 (1) Si/O - A Si/absorbed-monolayer of oxygen next to a thin epitaxial layer of silicon is used as the building block of a barrier to form a repeatable system, a superlattice. Since all transport properties depend on both the barrier height and the barrier width, and since the barrier width is dictated by the Si-O-Si thickness which cannot be changed, the formation of a superlattice by repeating the basic building block accomplishes the desired thickness of the barrier. Relatively thick barriers are used as
30 insulating devices including but not limited to SOI and thin barriers can be used in quantum devices.

(2) EpiSiO_x - A relatively thick EpiSiO_x layer consisting of SiO_x with x being

-13-

typically approximately 1 but variable from > 0 to 2 depending on application. This layer forms an epitaxial system on silicon on which epitaxial silicon, substantially free of defects such as stacking faults and dislocations can be

(3) Superlattice of EpiSiO_x - A thin layer of EpiSiO_x next to a thin layer of epitaxial silicon is used as the building block of a barrier to form a repeatable system, a superlattice. Since all transport properties depend on both the barrier height, which may be adjusted by controlling the oxygen content in the EpiSiO_x, and barrier width, and since the thickness of the EpiSiO_x layer can be varied, the formation of a superlattice by repeating the basic building block accomplishes the desired thickness and characteristics of the barrier. Relatively thick barriers are used as insulating devices including but not limited to SOI and thin barriers can be used in quantum devices.

(4) Multiple layers of EpiSiO_x with optional defect "reflection" layer - An insulating layer consisting of multiple layers of EpiSiO_x and epitaxial silicon deposited onto a silicon substrate (or epitaxial silicon surface). On top of the last EpiSiO_x layer a thick epitaxial device layer of silicon is deposited. This stacking of EpiSiO_x/epi-Si layers reduces the defect density generated in the final epitaxial device layer of silicon as a result of the "total" insulator layer. Additionally, any remaining defects can be further reduced by including a defect "reflection" layer of thin said barrier 30 to 50nm up from the insulating layer capped off with an epitaxial device layer of silicon. As a result, the final layer of epitaxial silicon will show a significant reduction in the number of defects. This procedure has been the basis of the patents:

(a) Blakeslee et al., U.S. Patent 4,088,515

(b) Blakeslee et al., U.S. Patent 4,278,474.

In accordance with the related art (Nakashima *et al*, ref. 21) in semiconductor applications and specifically for SOI applications the concentration of oxygen in each of the SiO_x layers can be increased by partially replacing oxygen with other elements including but not limited to C, N, P, Sb, or As. The elements can be introduced either during the oxygen deposition process, after the oxygen has been deposited, or later during the high temperature oxygen annealing step (described below and in ref. 21) in accordance with methods well understood by those skilled in the art. These elements act as traps, getters or diffusion barriers to trap extra oxygen in the oxide layer. Thereafter epitaxial silicon is deposited on the insulating oxide layer. In some applications, even

when above stated trapping/getting/diffusion elements are not used, after the epitaxial silicon is deposited, the structure can be annealed in an oxygen atmosphere according to Nakashima, allowing additional oxygen to penetrate through the epitaxial silicon into the oxide layer without introducing excess defects in the epitaxial silicon. Typical annealing
5 temperatures are 1300°C. ⁽²¹⁾

(1) Si/O

The quantum electronic concept was introduced by Esaki and Tsu 27 years ago,
^(1,2) first in man-made compound semiconductors called "Superlattices" and three years
later in resonant tunneling through quantum wells. These quantum devices require
10 epitaxial barriers, usually fabricated from III-V, or II-VI compound semiconductors, since
nearly matching the substrate lattice structures is important for the barrier formation. The
lack of such a barrier in silicon has prevented the extension of quantum devices to silicon
technology, and the search is on for a barrier for silicon. Said U.S. Patent No. 5,216,262
(1993), ⁽²²⁾ issued to R. Tsu described a method to build silicon-based quantum wells,
15 with a superlattice barrier structure consisting of thin silicon layers sandwiched between
monolayers of SiO₂.

In the present invention we have discovered a way to deposit and the resultant
structure of a monolayer of absorbed oxygen which contains less oxygen than is contained
in SiO₂. Oxygen is first introduced by absorption onto a clean silicon surface at
20 temperatures up to 700°C and high vacuum pressure ($< 10^{-6}$ torr). Because the absorption
process cannot exceed one monolayer under these controlled conditions, the method
serves as a self-limiting process, ensuring the thickness of oxide at a monolayer, which is
less than the amount of oxygen required to make a monolayer of SiO₂, thus allowing the
continuation of the Si epitaxial growth. Our present results have been obtained by using
25 standard MBE (Molecular Beam Epitaxy) monitored by RHEED (Reflection High Energy
Electron Diffraction). The epitaxial silicon sandwiched between two absorbed mono-
layers of oxygen forms a unit, which can be repeated to give a superlattice structure. The
barrier structure shows a barrier height of 0.5 eV, which is more than sufficient for most
electronic and optoelectronic devices at room temperature. Current voltage
30 measurements show the existence of a barrier, surface Auger shows the presence of
oxygen where expected, and high resolution X-TEM (cross section transmission electron
microscopy) shows almost defect free Epitaxy beyond the barrier layer. We name this

-15-

system consisting of monolayers of absorbed oxygen sandwiched between thin epitaxially grown silicon layers HES (Hetero-Epilattice Superlattice).

It is an important observation that the epitaxial growth of silicon can indeed be continued. We have not established, however, if the continuation of epitaxy is because
5 the absorbed oxygen provides less than full coverage, or because the oxygen at the interface forms a strain-layered oxide. If the coverage is not 100%, it is natural that silicon can establish epitaxy. Alternatively, a monolayer with full coverage of oxygen should not totally mask the potential function presented by the substrate silicon surface, thus allowing the re-establishment of epitaxy. Our present data favor the latter possibility
10 because we are able to bring back the epitaxial growth of silicon even after 100 L of oxygen (one L, Langmuir, is an exposure of oxygen at 10^{-8} Torr for 100 seconds). Although this theoretical issue is of a fundamental nature, the fact that a barrier forms regardless of the exact mechanism is the most important technical factor. More than twenty-five years ago, Distler, reported the oriented nucleation of gold on NaCl precoated
15 with an amorphous carbon layer below a critical thickness. Subsequently, Henning confirmed Distler's observation that a sufficiently thin amorphous intermediate layer between substrate and deposit failed to inhibit epitaxy. Our verification of epitaxy substantially free from defects is based on in-situ RHEED and ex-situ X-TEM measurements.

20 Absorption of oxygen on a clean reconstructed surface does not have sufficient energy to overcome the 0.25-0.3 eV activation barrier for the transformation from a 2-dimensional silicon clean surface to a disturbed 3-dimensional silicon surface. Few observable changes in RHEED are seen in the reconstructed clean silicon surface except for a "fading" of the secondary lines as a result of dimerization of the surface silicon.
25 However, once Si atoms arrive from the e-beam source, there is sufficient energy available to overcome the barrier resulting in a more 3D surface morphology. This is the reason why a minimum thickness of about 1 nm is needed for the silicon deposition to re-establish epitaxy.

(2) EpiSiO_x

30 Preferably a substrate of monocrystalline silicon is heated to a temperature of between 400° and 700°C in a deposition chamber, preferably below 650°C. Silicon and an impurity element are simultaneously introduced into the chamber by any method

generally known to those skilled in the art. In the preferred embodiment of the invention the impurity element is oxygen but other elements such as carbon and nitrogen as a pure gas or part of a gaseous compound which form an insulating barrier when combined with Si could be used. There are possible combinations of elements, which could be

5 introduced to form such an insulating barrier as well, including but not limited to oxygen and carbon, carbon and hydrogen or oxygen and nitrogen.

Some deposition methods typically used are chemical vapor deposition, sputtering and molecular beam epitaxy. In the preferred embodiment, a layer EpiSiO_x is deposited on a substrate of silicon (or alternately on epitaxial silicon) and the concentrations of

10 silicon and oxygen adjusted until optimum concentrations allow for the deposition of substantially defect free epitaxial silicon on the layer of EpiSiO_x . The thickness of the insulating layer can be controlled by the time, deposition rate of silicon and temperature. The insulating properties of the barrier can be controlled by adjusting the amount of oxygen exposure. Once the preferred thickness of insulating barrier has been deposited,

15 epitaxial silicon may be deposited on top of the insulating barrier producing a low defect layer of silicon for use in any of a number of methods used by those skilled in the art. Epitaxial silicon with less than 10^{11} defects per square centimeter can be grown on top of the insulating barrier, with typical defects of less than 10^{10} defects per square centimeter, providing device quality silicon on which to build conventional integrated circuits with

20 significantly reduced leakage current, photoelectric devices of silicon or devices containing quantum wells of silicon.

In one embodiment of the invention the silicon is deposited by electron beam epitaxy and oxygen is simultaneously introduced into the chamber in concentrations high enough to provide a quality insulating layer but low enough to insure that the oxide layer

25 is epitaxially grown. This is monitored by using RHEED to insure that the crystalline structure of the silicon substrate is maintained in the oxide layer. RHEED is used to adjust the oxygen pressure and the rate of deposition of silicon. When the concentration of oxygen is too high or the deposition rate of silicon too slow, the RHEED pattern changes to indicate a reduction of quality of the subsequent surface from what is

30 necessary to continue high quality epitaxial growth of silicon. The rate of silicon deposition can be measured with a 6 megahertz oscillating silicon crystal or any of a number of different methods. Typically oxygen pressure is 10^{-6} Torr, but it could be done

with other higher and lower oxygen pressures. Typical electron beam epitaxy silicon deposition rates are 0.4 Å/s using molecular beam deposition but these rates will vary depending on the process used. Chemical vapor deposition is one of a number of alternative methods of depositing the silicon and oxygen.

- 5 Typically the silicon substrate, on which the barrier is deposited, is kept at temperatures of 400° to 700°C in a vacuum chamber typically kept at a pressure of 10^{-6} Torr or less background pressure, however depending on the specific element introduced to form the insulating barrier these values will change.

- 10 Although the preferred embodiments of the present invention are described herein with oxygen as the element bonding to silicon to form an insulating layer, as will be recognized by those skilled in the pertinent art, this invention includes other elements to be bonded with silicon to form said insulating layer. In addition although details of the molecular beam epitaxy system used to prepare the insulating layer are described herein, as will be recognized by those skilled in the pertinent art, this invention includes other
15 methods of depositing silicon with at least one other element in a way to form an insulating barrier.

(3) Superlattice of EpiSiO_x

- 20 In a method as described in (2) above a very thin layer of EpiSiO_x is deposited on a monocrystalline silicon substrate or on epitaxial silicon. A thin layer of epitaxial silicon is deposited next to the first EpiSiO_x layer, which forms a building block for generating a superlattice of alternating layers of EpiSiO_x and epitaxial silicon. The resultant structure has many applications in semiconductor devices.

(4) Multiple layers of EpiSiO_x with optional defect "reflection" layer

- 25 Figure 8 shows one of the preferred embodiments of the current invention. There is evidence that the thicker the layer of EpiSiO_x the higher the number of dislocations in the epitaxial silicon above it. It is therefore another aspect of this invention to decrease the number of defects in the top layer (see Figure 8) of epitaxial silicon by using multiple thin layers of EpiSiO_x in place of one thick layer of EpiSiO_x. The thinner the layer of EpiSiO_x, the faster that the surface quality can be recovered. In Figure 8 thicknesses of 25
30 Angstroms separated by epitaxial layers of 100 Angstroms are shown for the preferred embodiment, but these thicknesses may vary. Thus by using multiple layers, the number of defects in the final top epi-layer can be reduced.

Even with such thin layers of EpiSiO_x sandwiched between epitaxial silicon, there will be some dislocations, which are manifested in the layer of epitaxial silicon grown on top of the last EpiSiO_x layer. It is a further optional disclosure of this invention to place an additional thick layer of epitaxial silicon (typically 300 to 500 angstroms as shown in Figure 8) on top of the last EpiSiO_x layer. By capping this thicker layer of silicon with a very thin layer (or series of layers sandwiched between thin layers of epitaxial silicon) of either EpiSiO_x or an absorbed oxygen monolayer, there is sufficient space to allow threading dislocations to be deflected and terminated inside this thick layer of silicon ⁽¹³⁾, significantly reducing the number of defects in the top layer of epitaxial silicon (see Figure 8).

In preferred embodiments of the invention a quantum well consists of monocrystalline silicon epitaxially grown between two said barrier sections. The barrier section consists of a region of alternate thin layers of Si and an oxygen enriched layer of Si (either EpiSiO_x with $0 < x < 2.0$ or a monolayer of oxygen). This structure exhibits all of the quantum confinement effects and is fully compatible with silicon technology.

In a preferred embodiment of the present invention, the quantum well structure for semiconducting devices comprises: first and second barrier regions each consisting of alternate layers of said barrier with thicknesses so thin that no defects can be generated as a result of the release of stored strain energy. This thickness is generally in the range of 2 to 4 monolayers. A much thicker section of pure silicon is sandwiched between this barrier regions service as quantum confinement of carriers. Note that the proposed barriers can also serve to confine the holes in the valence band. Doping either with modulation doping, i.e. only in the silicon layers in the barrier region or involving also the well region may be incorporated to form desired junction characteristics. Hydrogen may also be used to passivate some of the residual defects if necessary.

In a preferred embodiment of the invention, 3-dimensional IC devices can be constructed using said barrier between epitaxial layer of device grade silicon. IC devices are constructed in the individual silicon layers, which are connected within the layers and between the layers. Figure 7 shows a schematic illustration of how an insulating layer so deposited allows for epitaxial silicon to be grown on top of the insulator. The epitaxial silicon becomes the substrate for a new layer of IC devices, thus creating a three-dimensional integrated circuit. Interconnections between one layer and the next can be

-19-

done in any of a number of ways which might include appropriate doping, such as n^+ , of the epitaxial silicon to form conducting regions from one level of ICs to the next.

Examples of how said barrier can be used in some typical devices are shown in Figure 1B. In the drawings which show SiO_x as the replacement insulating layer it should be understood that SiO_x represents said barrier on the specific application. In addition Figure 1 schematically illustrates how an SOI (said barrier shown as *Insulator*) layer can be typically used in a CMOS Inverter application. Anyone skilled in the art will know how to use the insulating layers disclosed in this invention to extend the applications to other semiconductor devices.

10 The silicon MOSFET (FIG. 4) is probably the most important solid state electronic device. The oxide, amorphous SiO_2 , is sandwiched between a metal gate contact and silicon channel region of the device. The lower the interface defect density between the SiO_2 and silicon, the faster the switching speed. The replacement of the amorphous SiO_2 by said barrier described in this invention can reduce the interface defect
15 density between the silicon and the insulator. To be more precise, as shown in Fig. 5, the amorphous SiO_2 serving as the insulating layer between the metal gate and the silicon is now replaced with said barrier. Alternatively, as shown in Figure 6, a layer of SiO_2 can be used between the top layer of said barrier and the metal gate. In this configuration there will still be defects at the interface with SiO_2 but now these defects are located away
20 from the silicon, consequently not effecting the switching performance. Conventional epitaxial silicon growth techniques such as VPE (vapor phase epitaxy) with the use of gaseous sources such as SiH_4 , MBE (molecular beam epitaxy), sputtering, and CBE (chemical beam epitaxy) may be used to fabricate such structures.

CLAIMS

1. A method for producing an insulating or barrier layer, useful for semiconductor devices, on a silicon substrate, which comprises depositing a layer of silicon and at least one additional element on said silicon substrate whereby said deposited layer is
5 substantially free of defects such that epitaxial silicon substantially free of defects can be deposited on said deposited layer.
2. A method according to claim 1, wherein said additional element is selected from the group consisting of oxygen, carbon, nitrogen, phosphorus, sulfur, hydrogen, antimony and arsenic, and combinations thereof.
- 10 3. A method according to claim 1, wherein said additional element is oxygen.
4. A method according to claim 3, wherein said deposited layer comprises SiO_x wherein $0 < x < 2.0$.
5. A method according to claim 4, wherein silicon and oxygen are deposited simultaneously.
- 15 6. A method according to claim 1, wherein silicon and said at least one additional element are deposited simultaneously.
7. A method according to claim 1, wherein said deposited layer is essentially epitaxial.
8. A method according to claim 1, wherein the surface of said silicon substrate is
20 epitaxial.
9. A method according to claim 1, wherein a plurality of insulating layers are deposited to form a barrier comprising a plurality of insulating layers sandwiched between epitaxial silicon.
10. A method according to claim 9, wherein said additional elements comprise oxygen
25 and at least one other of said additional elements.
11. A method according to claim 10, wherein oxygen is diffused into said deposited layer and is trapped by said at least one other of said additional elements.
12. A method according to claim 11, wherein the produced barrier is annealed in an oxygen atmosphere.
- 30 13. A method according to claim 9, wherein the values of dielectric constant and barrier height of the produced barrier are adjusted to desired values by controlling the oxygen content of said barrier.

14. A method according to claim 9, wherein a barrier with a controlled gradient of oxygen content is produced by adjusting the oxygen content of said insulating layers.
15. A barrier composite useful for semiconductor devices, comprising an insulating layer of silicon and at least one additional element deposited on a silicon substrate
5 whereby said insulating layer is substantially free of defects, and a deposit of epitaxial silicon substantially free of defects deposited on said insulating layer.
16. A barrier composite according to claim 15, wherein said additional element is selected from the group consisting of oxygen, carbon, nitrogen, phosphorus, sulfur, hydrogen, antimony and arsenic, and combinations thereof.
- 10 17. A barrier composite according to claim 15, wherein said additional element is oxygen.
18. A barrier composite according to claim 17, wherein said insulating layer comprises SiO_x wherein $0 < x < 2.0$.
19. A barrier composite according to claim 15, wherein said insulating layer is
15 essentially epitaxial.
20. A barrier composite according to claim 15, wherein the surface of said silicon substrate is epitaxial.
21. A barrier composite according to claim 15, comprising a plurality of insulating layers forming a barrier comprising a plurality of insulating layers sandwiched between
20 epitaxial silicon.
22. A barrier composite according to claim 21, wherein said additional elements comprise oxygen and at least one other of said additional elements.
23. A semiconductor device comprising a barrier composite, said barrier composite comprising an insulating layer of silicon and at least one additional element deposited on
25 a silicon substrate whereby a deposit of epitaxial silicon substantially free of defects deposited on said insulating layer.
24. A semiconductor device according to claim 23, wherein said additional element is selected from the group consisting of oxygen, carbon, nitrogen, phosphorus, sulfur, hydrogen, antimony and arsenic, and combinations thereof.
- 30 25. A semiconductor device according to claim 23, wherein said additional element is oxygen.
26. A semiconductor device according to claim 25, wherein said insulating layer

-22-

comprises SiO_x wherein $0 < x < 2.0$.

27. A semiconductor device according to claim 23, wherein said insulating layer is essentially epitaxial.

28. A semiconductor device according to claim 23, wherein the surface of said silicon substrate is epitaxial.

29. A semiconductor device according to claim 23, comprising a plurality of insulating layers forming a barrier comprising a plurality of insulating layers sandwiched between epitaxial silicon.

30. A semiconductor device according to claim 29, wherein said additional elements comprise oxygen and at least one other of said additional elements.

31. A semiconductor device according to claim 26, wherein said semiconductor device comprises a structure selected from the group comprising resonant tunneling devices, single electron field effect transistors, quantum well devices, metal oxide semiconductor field effect transistors and integrated circuit devices.

32. A method for producing an insulating or barrier layer, useful for semiconductor devices, on a silicon substrate, which comprises absorbing on said silicon substrate one or more elements to form a monolayer of said element or elements, onto which can be grown epitaxial silicon.

33. A method according to claim 32, wherein said elements are selected from the group consisting of oxygen, carbon, nitrogen, phosphorus, antimony and arsenic, and combinations thereof.

34. A method according to claim 33, wherein said elements comprise oxygen.

35. A method according to claim 32, wherein the surface of said silicon substrate is epitaxial.

36. A method according to claim 32, wherein a plurality of insulating layers are deposited to form a barrier comprising a plurality of insulating layers sandwiched between epitaxial silicon.

37. A semiconductor device comprising a barrier as defined in claim 36.

38. A semiconductor device according to claim 37, wherein said semiconductor device comprises a structure selected from the group comprising resonant tunneling devices, single electron field effect transistors, quantum well devices, metal oxide semiconductor field effect transistors and integrated circuit devices.

1/6

FIG. 1A
CMOS - Typical

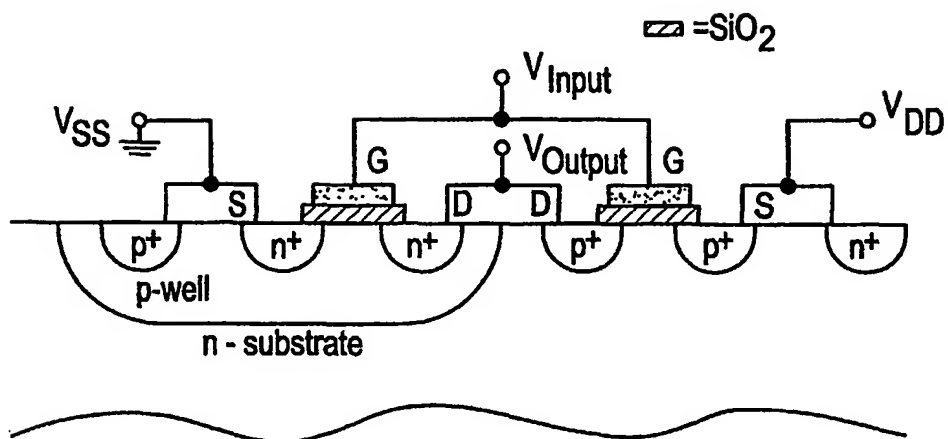


FIG. 1B
CMOS - EpiSiO_x/SOI

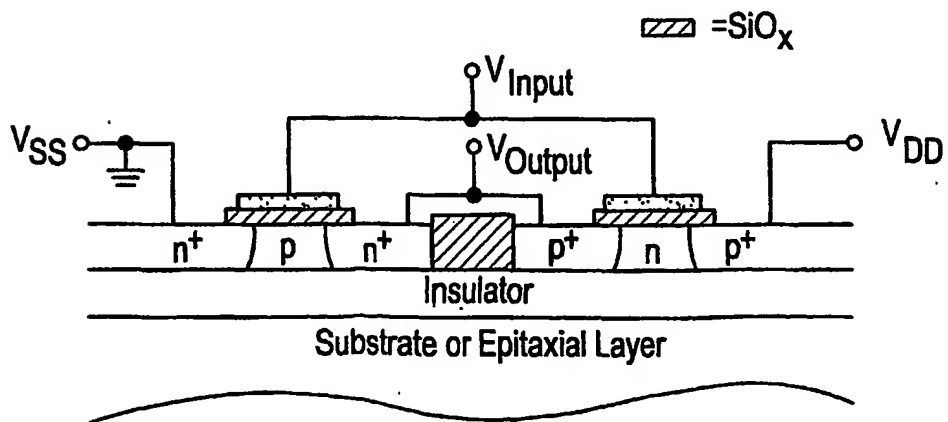


FIG. 2C

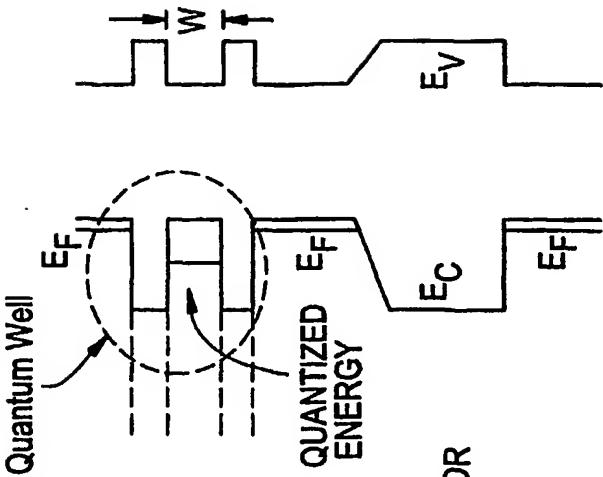


FIG. 2B

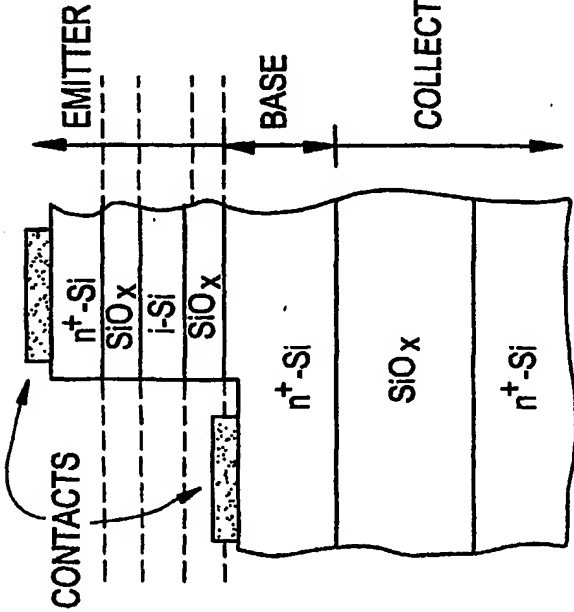
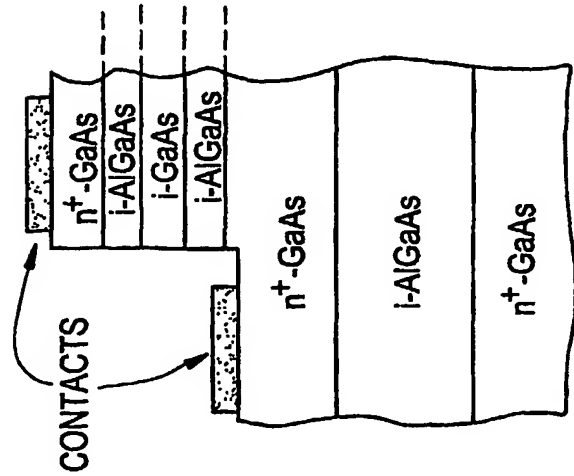


FIG. 2A



3/6

FIG. 3A

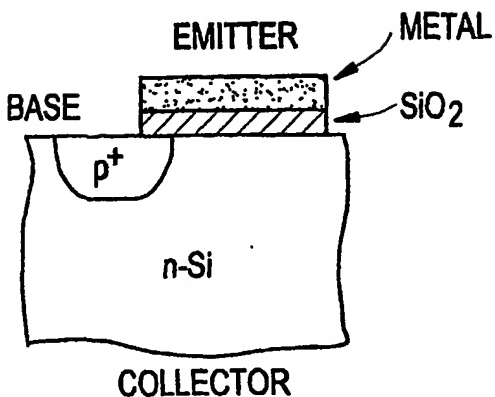


FIG. 3B

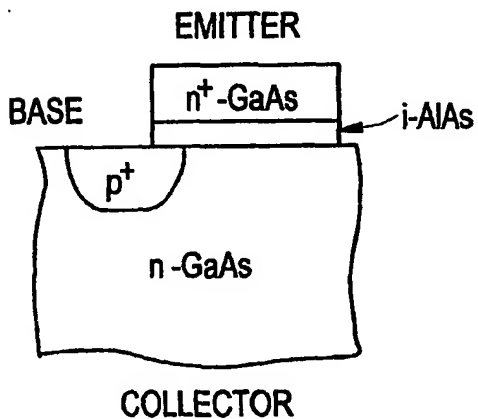
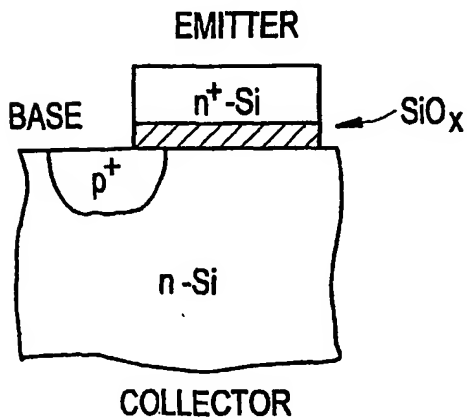


FIG. 3C



4/6

FIG. 4

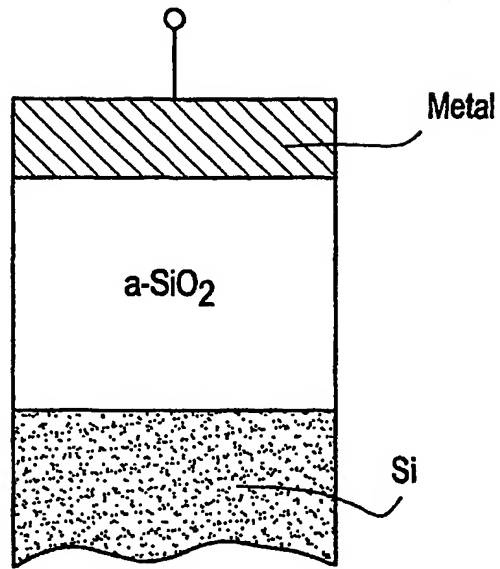


FIG. 5

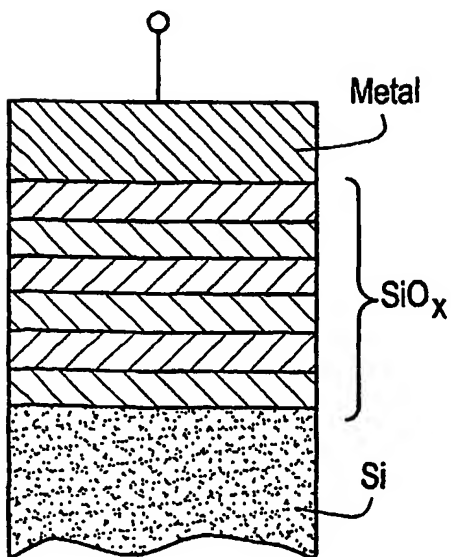
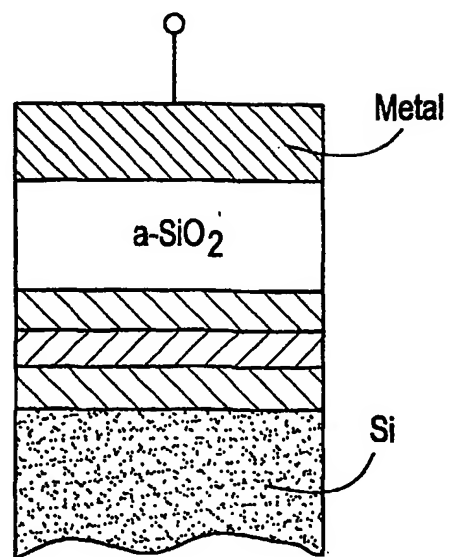


FIG. 6



5/6

FIG. 7

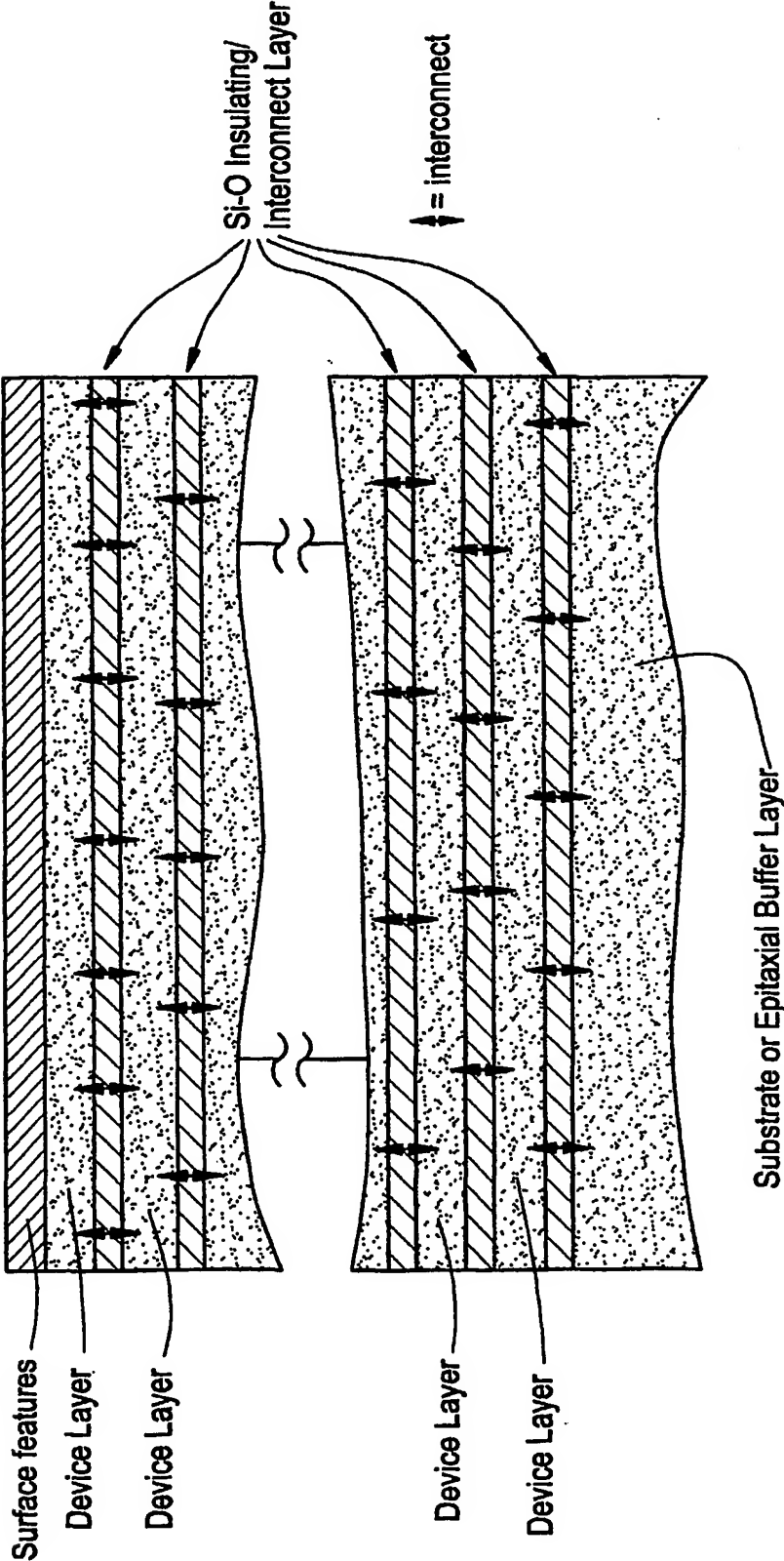
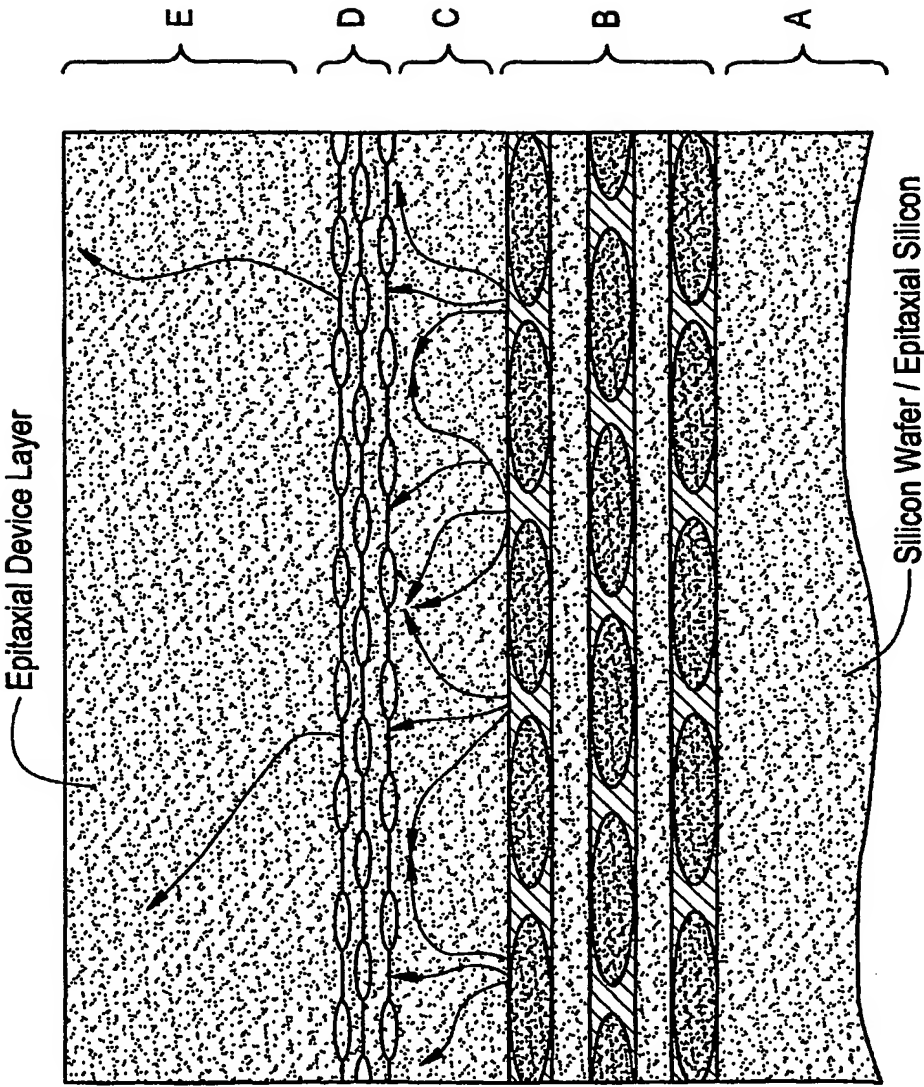


FIG. 8



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/40970**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(7) :H01L 21/20, 21/36, 21/339, 21/31, 21/469

US CL :438/149, 479, 787

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/149, 479, 787, 481, 778, 783, 784, 787; 257/15; 117/92, 103, 108

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONEElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	TSU et al. Visible electroluminescence in Si/adsorbed gas superlattice, Proceedings of the SPIE, 1997, Vol. 3290, pages 246-256, especially pages 249, 251.	1-4, 7, 8
X	TSU et al. Silicon Epitaxy on Si(100) with Adsorbed Oxygen, Electrochemical and Solid-State letters, April 1998, Vol. 1, Issue 2, pages 80-82.	1-3, 5, 6, 8, 15-17, 19-21, 23-25, 27-29, 32-34, 36-38
A	US 5,216,262 A (TSU) 01 June 1993 (01.06.1993), col. 2, lines 8-20.	1-38

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

20 AUGUST 2001

Date of mailing of the international search report

10 OCT 2001

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Facsimile No. (703) 305-3230

Authorized officer

CRAIG LYTTLE

Telephone No. (703) 308-1782

René Panton